

## Introduction to ASIC Design Industry

- [what is an ASIC](#)
- [Analogy of VLSI & Building Arch](#)
- [ASIC Design Flow](#)

## Architectural Discussions

- [Asking Before Architecting](#)
- [Touch base on Hardware & software co-designing](#)
- [Dog on duty: Watch Dog Timer \(Duty Dog in the Chip\)](#)
- [How to Design FIFO Depth](#)
- [what to look for when i receive a 3rd party delivery](#)

## Register Transfer Language Discussions

- [online verilog codes for logic like comparator/mux/flipflop/multiplier/subtractor..](#)
- [Good verilog coding styles](#)
- [Thoughts of an Good RTL designer](#)
- [Verilog Free Simulators download](#)
- [how to encrypt RTL IP synopsys friendly?](#)

## Chip Implementation Discussions

- [Chip Die size Estimation](#)
- [need for special cells while using multi-Vdd flow](#)
- [IBIS model Board level Signal Integrity](#)
- [Talk about Chip Crosstalk : Impacts, Issues, Methodology in Chip Design flow,](#)

### Precaution measures

- [IC Packaging](#)
- [what contributes towards Clock Insertion Delay/skew](#)
- [sources of power dissipation in CMOS](#)
- [what are the clock Tree constraints as a handoff to CTS designer](#)
- [how to build clock-mesh structures...](#)
- [Power saving mechanism's and their contribution in reducing power savings](#)
- [study about spare-cells](#)

## Chip Verification Strategies Discussions

- [Bus Architectures - Performance Boosters](#)
- [bus functional models \(transactors\)](#)
- [Murphys Law - Verification Methodologies \(insurance policies\)](#)

## Chip Design Synthesis & Timing Closure Discussions

- [Explains synthesis flow](#)
- [synopsys constraints template file](#)
- [What to look for to close timing faster](#)
- [What are the various timing arcs](#)
- [Concepts of Static Timing analysis](#)
- [Guideline for a Faster Timing closure](#)
- [On chip variation - Static Timing Analysis](#)
- [clock on demand: clock gating concept](#)
- [how to solve setup and hold violations](#)

## Chip Design For Test Discussions

- [Design for Test \[DFT\]](#)
- [List of Failure Analysis Tools](#)
- [Curve Tracer Measurement Tools: An Aid to Failure Analysis](#)

## Chip Manufacturing Discussions

- [what is Wafer Dicing?](#)